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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,897	03/30/2001	Zheng Luo	1125-CS	8975

7590 04/07/2004  
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EXAMINER

YANCHUS III, PAUL B

ART UNIT	PAPER-NUMBER
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2116

DATE MAILED: 04/07/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/821,897

Applicant(s)

LUO ET AL.

Examiner

Paul B Yanchus

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## DETAILED ACTION

### *Claim Objections*

Claim 15 is objected to because of the following informalities: Claim 15 contains a grammatical error in line 14. The word "of" should be inserted after the word "generation" in line 14 to correct the grammatical error. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ober, US Patent no. 6,665,802.

Regarding claims 1-3, Ober teaches a system on a chip comprising:

a first power plane for powering a core logic portion of the system on a chip [column 4, lines 13-15 and column 5, lines 38-40];

a second power plane for powering selected circuitry of the system on a chip [column 5, lines 38-50];

clock generation circuitry for generating clocks for clocking operations of selected circuits of the system on the chip in response to a signal generated by an oscillator [column 8, lines 53-64]; and

power control circuitry operable to:

in a first mode, switch-off power to the first [column 16, lines 9-16] and second power planes [subsystems 30-40, column 9, lines 49-55], the oscillator being enabled; and

in a second mode, disable the clock generation circuitry and switch power to the first [IDLE mode, column 15, lines 15-20 and column 9, lines 49-55] and second power planes [subsystems 30-40, column 9, lines 49-55], the oscillator being enabled.

Ober teaches a system on a chip intended for use in a cellular phone or similar device that contains other power planes [subsystems] besides the CPU core. The subsystems could be standard or application specific subsystems [column 1, lines 65-67 and column 5, lines 38-50]. Ober does not explicitly teach that one of the standard or application specific subsystems is an analog circuitry subsystem. However, it is well known in the art that conventional cellular phone devices have analog circuitry, such as a phase-locked-loop circuit and an A/D converter.

Regarding claims 4 and 5, Ober teaches that the CPU core logic comprises a microprocessor or a digital signal processor [column 5, lines 28-31].

Regarding claim 6, Ober, as described above, teaches a incorporating a plurality of standard or application specific subsystems on a system on a chip. Ober does not explicitly teach a pulse width modulator being included in one of the subsystems. However, pulse width modulators are well known to be used in cellular phone devices.

Regarding claim 7, Ober teaches an IDLE mode which pauses the execution of the CPU core by stopping the clock signal from being input to the CPU core [column 15, lines 15-23].

Regarding claim 8, Ober does not explicitly teach generating a signal to provide to an external switch for switching off power to the power planes. However, since the power supply

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for the system on a chip is externally located [see Figure 1], it would be obvious to one of ordinary skill in the art that the system would have to generate and provide a signal to an external switch to change the power supplied to various subsystems of system on a chip.

Regarding claim 9, Ober, as described above, teaches an apparatus for power control for a system on a chip system. Therefore, Ober also teaches the method performed by the apparatus. In addition, Ober also teaches selectively powering different power planes based on application requirements [column 9, lines 49-52].

Regarding claims 10, 11 and 14, Ober teaches entering deep sleep and sleep modes when the CPU core sets a flag in a power management register. The system will wake up from the sleep and deep sleep modes when an internal or external interrupt signal is received [column 16, lines 9-67].

Regarding claim 12, Ober, as described above, teaches an IDLE mode, which pauses the execution of the CPU core. In addition, Ober also teaches exiting the IDLE mode when an interrupt is received [column 15, lines 27-30].

Regarding claim 13, Ober teaches that the clock generation circuitry comprises a PLL [column 8, lines 53-64]. Ober also teaches powering down the PLL in order to disable clock generation and powering up the PLL in order to enable clock generation [column 16, lines 9-16].

Regarding claim 15-19, Ober, as described above, teaches a power control method and apparatus for a system on a chip.

Regarding claim 20, Ober teaches a I/O port subsystem that can have its power controlled independently from other subsystems [column 5, lines 42-43 and column 9, lines 49-53].

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Murakami et al., US Patent no. 6,542,982 teaches a cellular phone device with both digital and analog circuitry.

Voltz, US Patent no. 6,314,532, teaches a power management system for providing power to a plurality of independently operable devices.

Houston, US Patent no. 6,307,281, teaches a system for saving power by selectively applying power to different elements in the system.

Kannan et al, US Patent no. 5,511,205, teaches a computer system with individually controllable power planes.

JP 05109985 A teaches a system with independently powered functional units.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus  
March 31, 2004



THOMAS LEE  
SUPERVISORY PATENT EXAMINER  
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